A Fully Analytical AC Large-Signal Model of the GaAs MESFET for Nonlinear Network Analysis and Design

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Abstract—**In recent years much attention has been focused on nonlinear microwave circuit analysis. Several research groups have published new ideas and new approaches to more efficient computational schemes. To be able to apply these methods it is essential to have an accurate and efficient large-signal model for the device. In previous work the author has developed such a model for the GaAs MESFET. To further increase computational speed and to permit use of the model by other workers, a fully analytical approximation of the model was developed and is presented here. The accuracy of the model is demonstrated, and it is presented in a form that can be easily used and implemented by the reader.**

I. Introduction

THE TOPIC OF nonlinear microwave network analysis has been dealt with quite extensively in recent years, and practical methods have emerged for the efficient analysis of networks such as power amplifiers, mixers, and oscillators. There is no doubt that in the near future commercial computer programs for the analysis and design of nonlinear microwave networks will be widely used, much like programs for linear networks are used today. References [1]–[7] are just a sample of the publications on the above topics.

An essential prerequisite for the application of the above methods is the existence of a large-signal model for the nonlinear device. In this paper, such a model for the GaAs MESFET is dealt with. An efficient and accurate large-signal model was previously developed by the author [8], [9]. This model was applied to the analysis of several MESFET networks and shown to be accurate and efficient [11]–[13]. The above model is based on basic principles and is developed by the actual approximate solution of the field and charge transport differential equations. Therefore, the electrical performance is directly related to the device geometry and physical parameters.

The above model is "almost analytic" and therefore fast. However, due to the large size of the program, the actual circuit simulation is performed by the use of a pregenerated lookup table and an interpolation scheme.

This approach usually works quite well. However, convergence problems may occur sometimes during the optimization scheme since most optimization methods require continuous functions as well as continuous first derivatives. Also, the computer program to generate the lookup table is not presently available for public distribution.

In this paper we present a fully analytical large-signal model. This model is basically the same as above, except that the lookup table information is approximated by analytical expressions, most of which are designed to be continuous and possess continuous first derivatives. The advantages of this approach are a) better convergence of the optimization scheme and b) explicit expressions that can be readily applied by the reader.

In Section II a complete description of the model is presented. An investigation of the model accuracy by comparison to the previous model is described in Section III. The comparison includes simulation examples of a power amplifier and a mixer.

II. The Analytical Model

A. General

The MESFET large-signal model is presented in Fig. 1. The description of the various elements of the network is given in [8] and [9] with a modification by Green [10], except for CDG, CPAG, CPAD, which represent the capacitances between the three bonding pads of the device. Most of the elements in Fig. 1 are passive parasitic elements of the device, including the diodes that represent the source–gate and drain–gate junctions. The charge transport time delay via the channel is τ.

The active nonlinear portion of the device is represented by the box labeled "basic FET." This portion is characterized by a mathematical relationship between the two-port currents and voltages. As mentioned above, the mathematical expressions were developed by the actual solution of the field and transport differential equations. The expressions are

$$I_g = \mathrm{GVSG}\frac{dV_{SG}}{dt} + \mathrm{GVDS}\frac{dV_{DS}}{dt} \tag{1}$$

$$I_D = I_{\mathrm{con}} + \mathrm{DVSG}\frac{dV_{SG}}{dt} + \mathrm{DVDS}\frac{dV_{DS}}{dt}. \tag{2}$$

I_{con} is the drain–source conduction current. The other four variables are capacitive coefficients representing the displacement current of the device. The above five variables

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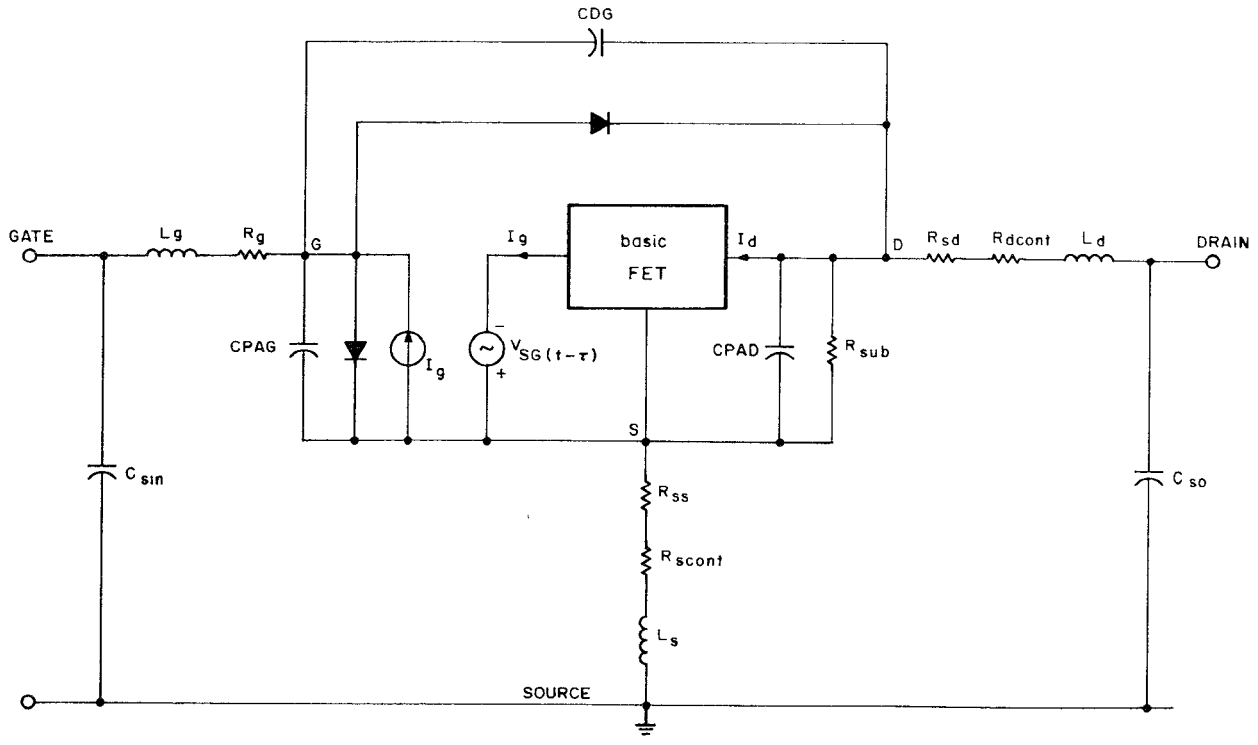

Fig 1. Complete MESFET network.

are functions of the port voltages V_{SG}, V_{DS}. These variables are computed by the computer model for a given pair of values for the voltages, as described in [8] and [9].

The computer model is used to generate a lookup table for the above five variables. In the actual large-signal analysis, the lookup table is used with an interpolation scheme.

In this paper we present analytical expressions for the above five variables. These expressions enable the reader to actually implement our model and verify the results. The expressions include 16 device parameters which must be supplied by the user, as outlined below. The expressions were derived by curve fitting to the lookup table data, such that most of the functions and the first derivatives are continuous.

B. The Conduction Current (I_{con})

The expressions for the conduction current are

$$I_{con} = \begin{cases} g_{d0}V_{DS} - \dfrac{g_{d0} - g_{ds}}{2V_{sat}} V_{DS}^2, & 0 \leq V_{DS} \leq V_{sat} \\ I_{sat} + 0.7 g_{ds} V_{sat}\left(1 - e^{-\left(\frac{V_{DS}}{V_{sat}} - 1\right)/0.7}\right), & V_{DS} > V_{sat}. \end{cases} \tag{3}$$

V_{sat} is the "knee voltage" and is calculated by

$$V_{sat} = \frac{2I_{sat}}{g_{ds} + g_{d0}}. \tag{4}$$

The three variables I_{sat}, g_{d0}, and g_{ds} are functions of V_{SG}. I_{sat} is the conduction current at $V_{DS} = V_{sat}$; g_{d0} and g_{ds} are the values of the drain conductance g_d at $V_{DS} = 0$ and at $V_{DS} = V_{sat}$, respectively.

The expressions for the above three functions are

$$I_{sat} = \begin{cases} I_{ON}, & V_{SG} < -V_F \\ A_1 V_{SG}^3 + A_2 V_{SG}^2 - g_{m0} V_{SG} + I_{DSS}, & -V_F \leq V_{SG} \leq 0 \\ A_3 V_{SG}^4 + A_4 V_{SG}^3 + A_5 V_{SG}^2 - g_{m0} V_{SG} + I_{DSS}, & 0 \leq V_{SG} \leq V_{cut} \\ 0, & V_{SG} \geq V_{cut} \end{cases} \tag{5}$$

where

V_F turn-on voltage of the gate–source junction ($\simeq$ 0.7 V),

V_{cut} cutoff voltage of the device (practically equal to the pinchoff voltage: V_p),

I_{ON} maximum drain current (open channel),

g_{m0} value of transconductance g_m for $V_{SG} = 0$, $V_{DS} = V_{sat}$

I_{DSS} I_{con} value for $V_{SG} = 0$, $V_{DS} = V_{sat}$.

The expressions for A_1 to A_5 are presented in the Appendix.

$$g_{d0}=\begin{cases} G_{dom}, & V_{SG}<-V_F \\ \dfrac{G_{doo}-G_{dom}}{V_F^2}V_{SG}^2+\dfrac{2(G_{doo}-G_{dom})}{V_F}V_{SG}+G_{doo}, & -V_F\leqslant V_{SG}\leqslant 0 \\ \dfrac{G_{doo}}{V_{\text{cut}}^2}V_{SG}^2-\dfrac{2G_{doo}}{V_{\text{cut}}}V_{SG}+G_{doo}, & 0\leqslant V_{SG}\leqslant V_{\text{cut}} \\ 0, & V_{SG}>V_{\text{cut}} \end{cases} \tag{6}$$

where

G_{doo} value of g_d for $V_{DS}=V_{SG}=0$,
G_{dom} value of g_d for $V_{DS}=0$, $V_{SG}=-V_F$.

$$g_{ds}=\begin{cases} 0, & V_{SG}<-V_F \\ C_1V_{SG}^3+C_2V_{SG}^2+C_3V_{SG}+C_4, & -V_F\leqslant V_{SG}\leqslant V_{gdsm} \\ D_1V_{SG}^3+D_2V_{SG}^2+D_3V_{SG}+D_4, & V_{gdsm}<V_{SG}\leqslant V_{\text{cut}} \\ 0, & V_{SG}>V_{\text{cut}}. \end{cases} \tag{7}$$

Here V_{gdsm} is the value of V_{SG} at which g_{ds} is maximum. Usually V_{gdsm} is the edge of the "almost linear" region of the device, so that for $V_{SG}>V_{gdsm}$, I_{con} decreases fast (decrease in g_m close to V_{cut}). *V_{gdsm} can be approximated by the constant V_p^{oo} in* [8] and [9]. *All the above parameters can be extracted from the static I–V curves of a given device.*

The expressions for C_1 to C_4 and D_1 to D_4 are presented in the Appendix.

C. Displacement Current Coefficients

In this subsection the expressions for the four displacement current coefficients are presented.

1) *GVSG*: This coefficient is the largest and most important capacitive function. In fact, this is approximately the common-source input capacitance of the device. It is practically independent of V_{DS}:

$$\text{GVSG}=\begin{cases} \text{GVSG}(-V_F), & V_{SG}\leqslant -V_F \\ \dfrac{C_0}{\sqrt{1+V_{SG}/\phi}}, & -V_F<V_{SG}\leqslant V_{\text{cut}} \\ \text{GVSG}(V_{\text{cut}}), & V_{SG}\geqslant V_{\text{cut}}. \end{cases} \tag{8}$$

C_0 is the value of GVSG for $V_{SG}=0$. *The user can specify here the input capacitance at $V_{SG}=0$ (not including the capacitance of the parasitic elements, of course).* ϕ is the built-in potential of the gate–source junction ($\phi\simeq 0.8$ V).

2) *GVDS*: This coefficient represents the active feedback capacitance (effect of dV_{DS}/dt on gate displacement current):

$$\text{GVDS}=C_k+\frac{C_m-C_k}{1-\tanh(-1)}\left[1-\tanh\left(2\frac{V_{DS}}{V_{\text{sat}}}-1\right)\right], \quad V_{DS}\geqslant 0. \tag{9}$$

C_k is the value of GVDS for large V_{DS} (independent of V_{SG}).

The feedback capacitance for normal bias conditions ($V_{DS}>V_{sat}$) may be used here (usually supplied by the manufacturer in the small-signal equivalent circuit):

$$\begin{aligned} C_m&=\frac{C_{m0}}{\sqrt{1+V_{SG}/\phi}}, && -V_F\leqslant V_{SG}\leqslant V_{\text{cut}} \\ C_m&=C_m(V_{\text{cut}}), && V_{SG}>V_{\text{cut}} \\ C_m&=C_m(-V_F), && V_{SG}<-V_F \end{aligned} \tag{10}$$

where C_{m0} is the value of GVDS for $V_{DS}=V_{SG}=0$. *The term $\tanh(-1)$ ($=0.761$) is kept in* (9) (*and also in* (11) *and* (12) *below*) *to emphasize the meaning of the parameters C_m, C_k, etc. C_{m0} may be taken to be approximately one half of C_o.*

Practically, for normal bias and signal conditions, V_{DS} is above V_{sat} at all times. *In that case GVDS may be approximated by a constant C_k.*

3) *DVSG*: This coefficient represents the active feedback capacitance (effect of dV_{SG}/dt on drain displacement current). Its value is practically very small (around two orders of magnitude below GVSG and one order of magnitude below GVDS. *So, in practice it is possible to neglect it without any visible error.* However, for the sake of completeness, an analytical approximation is presented for it as well:

$$\text{DVSG}=-\left[C_{\max}-\frac{C_{\max}}{1-\tanh(-1)}+\frac{C_{\max}}{1-\tanh(-1)}\cdot\tanh\left(2\frac{V_{DS}}{V_{\text{sat}}}-1\right)\right], \quad V_{DS}\geqslant 0 \tag{11}$$

where $C_{\max}$ is the value of $(-\text{DVSG})$ for large V_{DS}.

4) *DVDS*: This coefficient represents the output capacitance:

$$\text{DVDS}=C_H-\frac{C_H-C_L}{1-\tanh(-1)}+\frac{C_H-C_L}{1-\tanh(-1)}\cdot\tanh\left(2\frac{V_{DS}}{V_{\text{sat}}}-1\right), \quad V_{DS}\geqslant 0 \tag{12}$$

where C_H is the DVDS value for large V_{DS} (practically independent of V_{SG}), and C_L is the DVDS value for $V_{DS}=0$ (practically independent of V_{SG}). For normal bias and signal conditions $V_{DS}>V_{\text{sat}}$, *and DVDS can be approximated by a constant (C_H).* C_H can be extracted from the small-signal equivalent circuit of the device (usually

TABLE I
NE720 PHYSICAL AND GEOMETRICAL PARAMETERS

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MESFET CASE 20 DEVICE PARAMETERS TABLE

    1) GATE-SOURCE SEPERATION (LGS): 1.00 MICRONS
    2) GATE LENGTH (LG): 1.00 MICRONS
    3) GATE-DRAIN SEPERATION (LGD): 1.00 MICRONS
    4) GATE WIDTH (W): 400.00 MICRONS
    5) DOPING LEVEL (ND): 3.00E+17 CM-3
    6) CRITICAL ELECTRIC FIELD (EC): 2.50 KV/CM
    7) SATURATED ELECTRON VELOCITY (VS): 1.00E+07 CM/SEC
    8) RELATIVE DIELECTRIC CONSTANT (ER): 12.50
    9) BUILT-IN POTENTIAL (PHB): .800 VOLTS
   10) GATE METALLIZATION RESISTANCE (RG): 2.000 OHMS
   11) SUBSTRATE LEAKAGE RESISTANCE (RSUBST): 5.00E+02 OHMS
   12) EPITAXIAL LAYER THICKNESS (A): .1350 MICRONS
   13)SOURCE METALLIZATION RESISTANCE(RSCONT):1.0000HMS
   14)DRAIN METALLIZATION RESISTANCE(RDCONT):1.0000HMS
MESFET CASE 20 PACKAGE/CIRCUIT PARAMETERS:
    1) CHARACTERISTIC IMPEDANCE (ZO): 50.0 OHMS
    2) SOURCE INDUCTANCE (SIND): 1.70E-01 NANOHENRIES
    3) GATE INDUCTANCE (GIND): 3.50E-01 NANOHENRIES
    4) DRAIN INDUCTANCE (DIND): 4.00E-01 NANOHENRIES
    5) PARASITIC INPUT CAPACITANCE (SCAPIN): 1.50E-01 PICOFARADS
    6) PARASITIC OUTPUT CAPACITANCE (SCAPO): 1.50E-01 PICOFARADS
    7)GATE PAD CAPACITANCE(CPADG): 1.00E-02PICOFARADS
    8)DRAIN PAD CAPACITANCE(CPADD): 1.00E-02PICOFARADS
    9)DRAIN TO GATE PAD CAPACITANCE(CAPDG): 1.00E-02PICOFARADS
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TABLE II
NE720 ELECTRICAL PARAMETERS FOR ANALYTICAL MODEL

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MESFET CASE 20 DEVICE PARAMETERS TABLE

    1) FORWARD CONDUCTION VOLTAGE(VF): .75 VOLT
    2) CUTOFF VOLTAGE(VCUT): 3.10 VOLT
    3) VSG FOR MAX GDS(VGDSM): 1.75 VOLT
    4) BUILT-IN POTENTIAL(PHI): .80 VOLT
    5) DEVICE MAX CURRENT(CURON): 165.0 MA
    6) DEVICE CURRENT FOR VSG=0(CURDSS): 115.0 MA
    7) GM FOR VSG=0(GMO): 50.00 MMHO
    8) MAX VALUE OF GD AT VDS=0(GDOM): 939.00 MMHO
    9) GD VALUE FOR VSG=VDS=0(GDOO): 527.00 MMHO
   10) GDS VALUE FOR VSG=VGDSM(GDSM): 4.000 MMHO
   11) GVSG VALUE FOR VSG=0(CO): .718 PF
   12) GVDS VALUE FOR VDS=VSG=0(CMO): .3500 PF
   13)(-DVSG) VALUE FOR LARGE VDS(CMAX) .0060 PF
   14)DVDS VALUE FOR LARGE VDS(CH) .0440 PF
   15)DVDS VALUE FOR VDS=0(CL) .0050 PF
   16)GVDS VALUE FOR LARGE VDS(CK) .0440 PF
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supplied by the manufacturer), and its value is close to that of C_k. C_L is approximately an order of magnitude smaller than C_{II}.

III. Analytical Model Accuracy Evaluation

A. General

In this section the evaluation of the analytical model accuracy is presented. Two types of accuracy tests were performed: (a) comparison of the analytical expressions with the values from the lookup table [8], [9] for a given device and (b) simulation of an amplifier and a mixer performance using the analytical expressions versus the lookup table. These tests are outlined below.

B. Analytical Expressions versus Lookup Table

The device used for the comparison tests is an NE720 MESFET, made by the NEC Corporation. The device physical parameters used for the lookup table calculation are listed in Table I. The device electrical parameters used for the analytical expressions are listed in Table II (for the meaning of the physical parameters, see [8] and [9]).

Since the most important parameters of the MESFET performance are the conduction current (I_{con}) and the function GVSG, these two functions versus V_{SG} and V_{DS} are used for the comparison. In Fig. 2 the function I_{con},

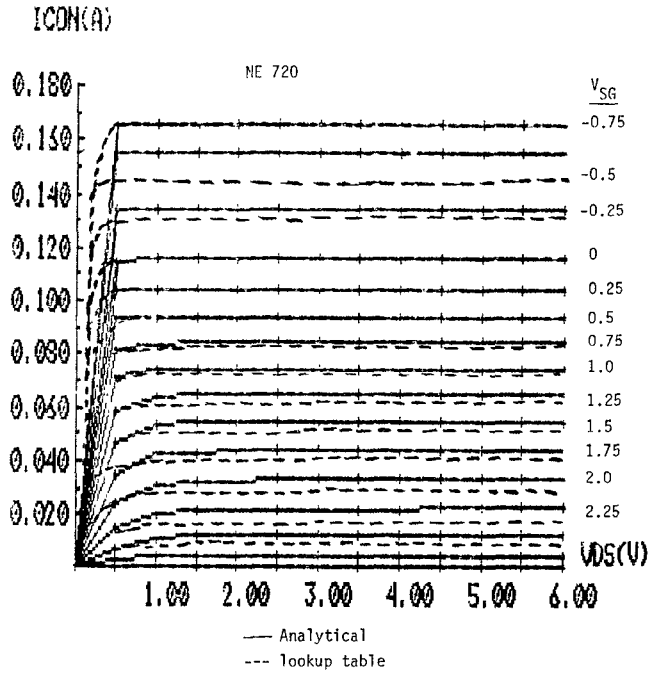

Fig. 2. Function I_{con} for analytical (solid) and lookup table (dashed).

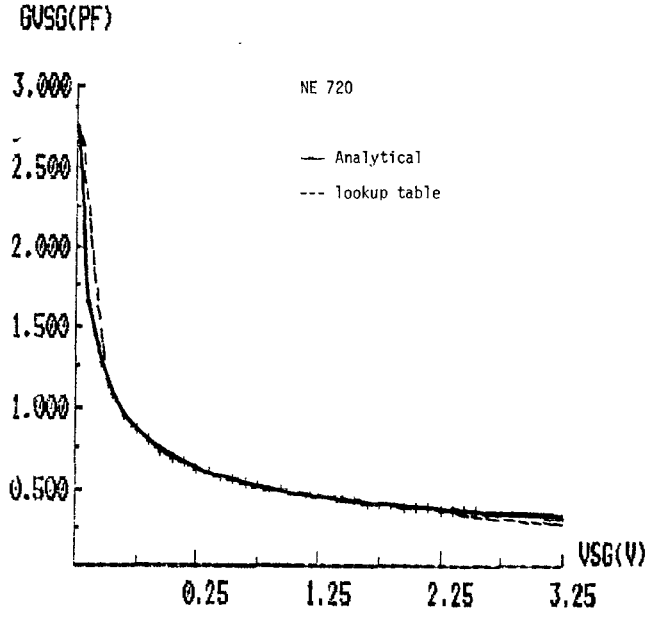

Fig 3 Function GVSG for analytical (solid) and lookup table (dashed).

which represents practically the static $I-V$ curves of the device, is presented for both the analytical expressions (solid line) and the lookup table (dashed line). From the figure it is obvious that generally there is good matching. There is some difference for $V_{SG} = -0.5$ and for low V_{DS} ($V_{DS} < V_{\text{sat}}$). The difference in the low V_{DS} range is simply due to the "piecewise linear" approximation for charge carrier velocity versus electric field function used in the numerical model [8], [9], compared to the parabolic approximation for I_{con} versus V_{DS} for the analytical expressions.

In Fig. 3 the function GVSG versus V_{SG} is presented for the analytical expressions (solid line) and the lookup table

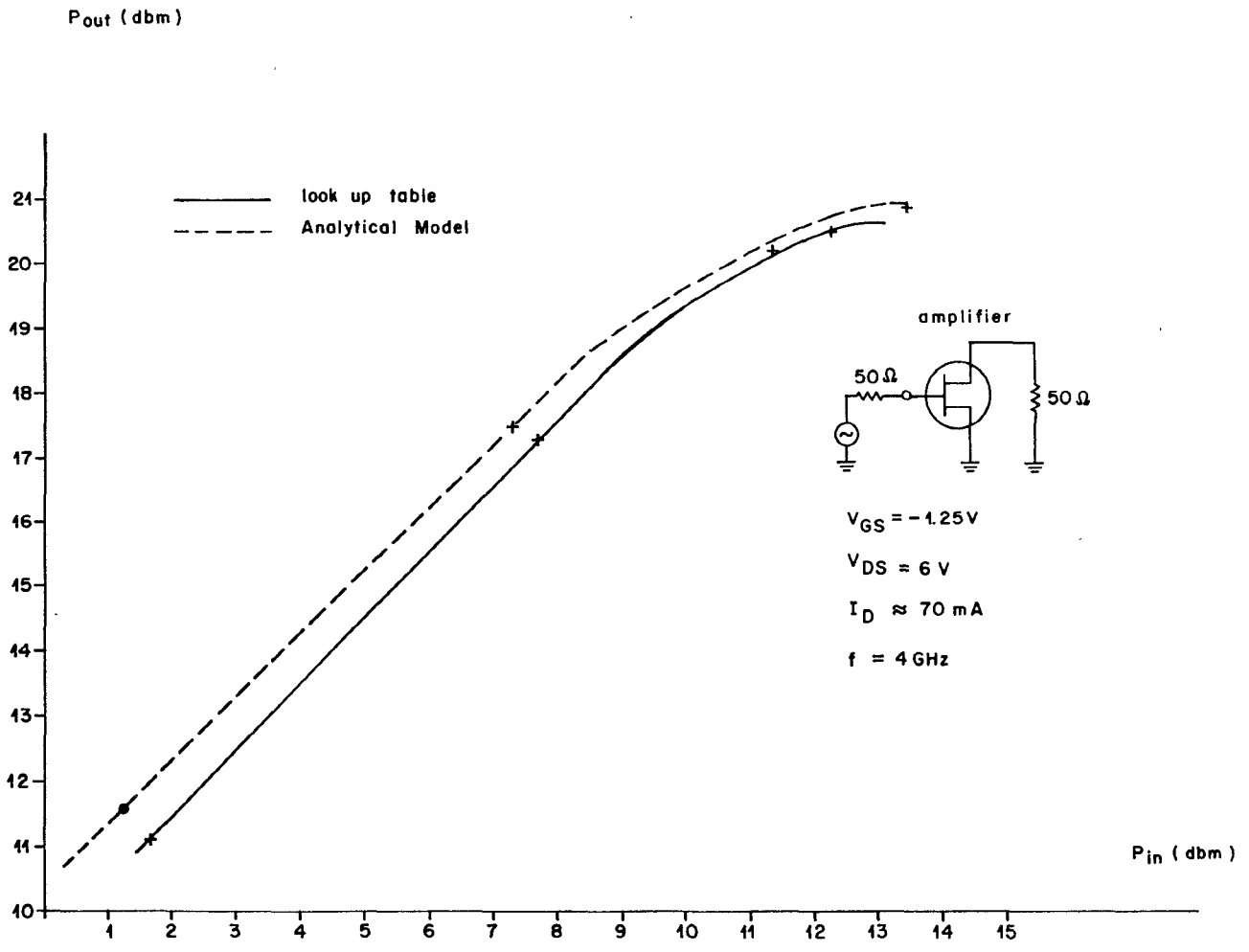

Fig. 4. Output power versus input power for an FET amplifier.

(dashed line). This function is practically independent of V_{DS}. From the figure it is obvious that there is very good agreement, except for a slight difference in the overdriven region ($V_{SG} = 0.75$).

C. Simulation Examples

The best accuracy test is the actual simulation of a large-signal network, and comparison of the performance using the two approaches. *Since the accuracy of the lookup table approach has already been proven by us for several networks — amplifier, mixer, oscillator* (*see* [11]–[13]), *it is sufficient to compare the two simulation results.*

The first network simulated is an amplifier made up of an NE720 device in common-source configuration excited by a 50-Ω source at the gate and loaded by a 50-Ω load at the drain. No attempt was made to optimize the circuit performance. The frequency is 4 GHz and the bias conditions are $V_{SG} = -1.25$ V, $V_{DS} = 6$ V. In Fig. 4 the output power of the amplifier versus the input power is presented for the analytical expressions (dashed line) and lookup table (solid line). From the figure it is obvious that there is quite good agreement between the two graphs.

The second network simulated is a MESFET mixer using the NE720 device in common-source configuration. The device is excited by 50-Ω RF and LO sources at the gate. The IF is extracted at the drain with a 50-Ω IF load. The gate is shorted for the IF frequency and the drain is shorted for the RF and LO frequencies. Up to eight LO harmonics are considered. All the frequencies generated in the device (except LO, RF, IF) are 50-Ω loaded at the gate and shorted at the drain. The analysis approach of the mixer uses the harmonic balance method and is outlined in [13]. The LO frequency is 4 GHz the RF frequency is 4.2 GHz. The bias conditions are $V_{GS} = -2.5$ V, $V_{DS} = 4$ V.

The available small-signal conversion gain of the mixer versus the LO power is presented in Fig. 5 (analytical–dashed line; lookup table—solid line). The good agreement between the two curves is obvious.

For the above large-signal simulations, the computations using the analytical model were approximately 25 percent faster than the computations based on the lookup table.

IV. Conclusions

In this paper a fully analytical version of an ac large-signal model for the GaAs MESFET is presented. The source model is a previously developed model based on basic principles and the actual physics and geometry of the device. The analytical version was developed by curve fitting the analytical expressions to the source model. The

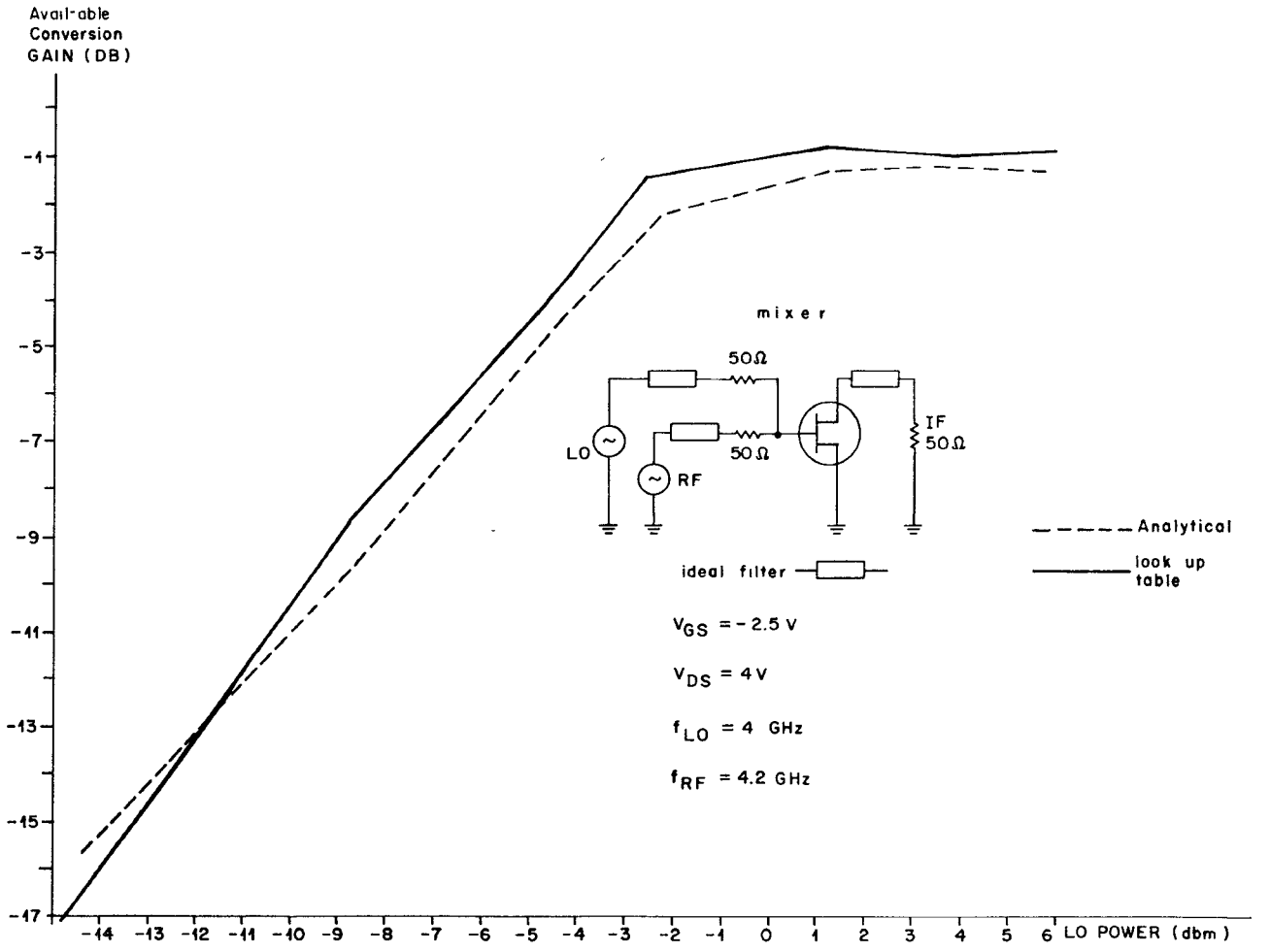

Fig. 5. Conversion gain of a MESFET mixer versus LO power.

analytical expressions presented here can be readily applied by the reader.

Appendix

In this appendix the expressions of several polynomial coefficients are presented.

The five coefficients for the I_{sat} expressions are

$$A_1 = \frac{2(I_{ON} - I_{DSS})}{V_F^3} - \frac{g_{m0}}{V_F^2}$$

$$A_2 = \frac{3(I_{ON} - I_{DSS})}{V_F^2} - \frac{2g_{m0}}{V_F}$$

$$A_3 = \frac{g_{m0}V_{\text{cut}}(2V_{\text{cut}} - 3V_{gdsm}) + 3I_{DSS}(2V_{gdsm} - V_{\text{cut}})}{V_{\text{cut}}^3\left[-V_{\text{cut}}^2 + 6V_{\text{cut}}V_{gdsm} - 6V_{gdsm}^2\right]}$$

$$A_4 = \frac{g_{m0} - 4V_{\text{cut}}A_3(V_{\text{cut}}^2 - 3V_{gdsm}^2)}{3V_{\text{cut}}(V_{\text{cut}} - 2V_{gdsm})}$$

$$A_5 = -6A_3V_{gdsm}^2 - 3 \cdot A_4V_{gdsm}.$$

The coefficients for the g_{ds} expressions are

$$C_1 = \frac{-2G_{dsm}}{(V_{gdsm} + V_F)^3} \qquad C_2 = \frac{3(V_{dgsm} - V_F)G_{dsm}}{(V_{gdsm} + V_F)^3}$$

$$C_3 = \frac{6V_{gdsm}V_FG_{dsm}}{(V_{gdsm} + V_F)^3} \qquad C_4 = \frac{V_F^2(V_F + 3V_{gdsm})}{(V_{gdsm} + V_F)^3}G_{dsm}$$

$$D_1 = \frac{2G_{dsm}}{(V_{\text{cut}} - V_{gdsm})^3} \qquad D_2 = \frac{-3(V_{gdsm} + V_{\text{cut}})G_{dsm}}{(V_{\text{cut}} - V_{gdsm})^3}$$

$$D_3 = \frac{6V_{gdsm}V_{\text{cut}}G_{dsm}}{(V_{\text{cut}} - V_{gdsm})^3} \qquad D_4 = \frac{V_{\text{cut}}^2(V_{\text{cut}} - 3V_{gdsm})}{(V_{\text{cut}} - V_{gdsm})^3}G_{dsm}.$$

The meanings of all the parameters used in the above expressions are presented in the text.

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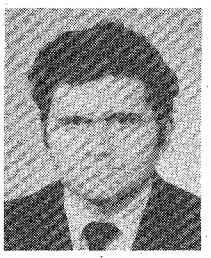

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Dr. Madjar has been serving for several years as AP/MTT joint chapter chairman in Israel. Since 1985 he has served as IEEE Israel section secretary.